UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,021	07/09/2003	Jri Lee	G&C 30448.116-US-U1	1118

22462   7590   02/21/2007

GATES & COOPER LLP
HOWARD HUGHES CENTER
6701 CENTER DRIVE WEST, SUITE 1050
LOS ANGELES, CA 90045

EXAMINER
WONG, LINDA

ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>27 November 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 11-16* is/are rejected.

7)☒ Claim(s) *7-10 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see Applicant's Remarks, filed 11/27/2006, with respect to the rejection(s) of claim(s) 1-20 under Wurzer et al (Publication: "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silcon Bipolar Technology") in view of Shimoda (US Patent No.: 5373257) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Song et al (Publication: "A 4-gb/s Clock and Data Recovery Circuit Using Four-Phase 1/8-Rate Clock") in view of Shimoda (US Patent No.: 5373257).

Claim Objections

2. **Claims 1,11** are objected to because of the following informalities:

    a. **Claims 1,11, lines 3,5,6,** recites the limitation "10Gb/s clock signal". Based on the specification, the units for the clock signal is "10GHz".

    Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-6,1-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Song et al (Publication: "A 4-gb/s Clock and Data Recovery Circuit Using Four-

Phase 1/8-Rate Clock") in view of Shimoda (US Patent No.: 5373257).

a. **Claims 1,11,**

    i.   Song et al discloses

- "a multi-phase voltage-controlled oscillator (VCO) for accepting a

  control signal and for changing a frequency of a clock signal output

  from the voltage-controlled oscillator in response thereto, wherein the

  voltage-controlled oscillator outputs a plurality of phases of the clock

  signal" (Fig. 1, label LPF outputs a control signal to label VCO, label

  VCO is shown to output a plurality of phases of the clock signal, Fig. 2,

  pp 240, right Col., lines 22-30)

- "a phase detector (PD) for sampling an input data signal using the clock

  signal received from the voltage-controlled oscillator and generating

  four output data signals in response thereto, wherein the input data

  signal is re-timed and de-multiplexed into the output data signals by the

  phase detector using the half-quadrature phase offsets of the clock

  signal, such that each of the output data signals detects an edge or

  transition in the input data signal and whether the edge or transition is

  early or late with respect to its corresponding half-quadrature phase

  offset of the clock signal" (Fig. 1, label four phase detector receives

  outputs from label VCO, Fig. 1, label 1:4 demultiplexed recovered data

shows four output data signals, Fig. 3 shows a phase detector for

retiming and demultiplexing the input data signal, Din, into the output

data signals, D0-D3, Fig. 4 shows the operation of the four-phase

detector and the edges or transitions are early or late, wherein the

edges or transitions detected depend on the clocks Ck0-Ck3 as

outputted from the VCO shown in Fig. 1 and Section B. Four-Phase

Detector, lines 1-11.)

- "a loop filter (LPF) for integrating the control current and for outputting

  the control signal to the voltage-controlled oscillator in response

  thereto" (Fig. 1, label LPF)

- "wherein the multi-phase voltage-controlled oscillator, phase detector,

  voltage-to-current converter and loop filter are implemented in

  complementary metal-oxide semiconductor (CMOS)". (Abstract

  discloses CMOS technology)

ii. Song et al fails to disclose

    A. A 10GHz clock signal with multiple phases outputted from the VCO

    B. A 40Gb/s data signal inputted into the phase detector

    C. A voltage-to-current (V/I) converter for converting the 10 Gb/s

       output data signals from the phase detector to a control current;

       and

    D. LPF integrating the control current from the voltage-to-

       current Converter

iii.   Regarding limitation A, although Song et al only discloses a .5Ghz four

phase clocks outputted by the VCO, it would have been obvious to one

skilled in the art at the time of the invention to produce multiple phases of a

10GHz instead of a .5GHz clock signals based on design choice.

iv.   Regarding limitation B, although Song et al only discloses a 4Gb/s data

signal inputted into the phase detector, it would have been obvious to one

skilled in the art at the time of the invention to input 40Gb/s data signal

instead of a 4Gb/s based on design choice.

v.   Regarding limitations C and D, Shimoda discloses such limitations as

stated above. (Fig. 2, labels 13-17) It would have been obvious to one

skilled in the art at the time of the invention to replace the charge pump and

LPF as disclosed by Song et al with a V/I converter and LPF as disclosed

by Shimoda to adjust the damping factor of the phase synchronizaztion loop

without destabilizing the operation by changing the control voltage of the

VCO so to adjust the frequency of the output signal of the VCO. (Col. 3,

lines 1-10, 32-40, Col. 2, lines 5-24 and lines 59-68, Col. 5, lines 33-39)

b. **Claims 2 and 12**, Song et al disclose "receiving a single input data signal and

retiming and demultiplexing the input data signal to a plurality of output data

signals". (Fig. 1, labels D0-D3, Fig. 3, Section B. Four-Phase detector)

c. **Claims 4 and 14**, Song et al disclose "a phase detector comprises a plurality of

flip-flops to strobe the input signal at intervals based on the plurality of phases

of the clock signal received from the VCO." (Fig. 3 shows flip-flops controlled

by CK0-Ck3 to strobe the input data signal, Din)

d. **Claims 3 and 13**, Song et al discloses "the phase detector uses half-quadrature

phases of the clock signal provided by the voltage-controlled oscillator to

sample the input data signal, thereby detecting the edges or transitions in the

input data signal, and determining whether the clock signal is early or late".

(Section B. Four-Phase Detector discloses a phase detector, which detects the

edges or transitions depending on 4 phase clock signals or half-quadrature

phases of the clock signal shown in Fig. 3.)

e. **Claims 5 and 15**, Song et al discloses "the phase detector compares every two

adjacent or consecutive samples stored by two adjacent or consecutive flip

flops by means of a XOR gate, which generates a difference or net output

current if the two consecutive samples are unequal, thus indicating the edge or

transition has occurred in the data signal". (Fig. 4)

f. **Claims 6 and 16**, Song et al shows in Fig. 4 the transitions or edges in which

are used to sample the input data signal based on the clock signals. (Fig. 4)

Allowable Subject Matter

4. **Claims 7-10,17-20** are objected to as being dependent upon a rejected base claim,

but would be allowable if rewritten in independent form including all of the limitations

of the base claim and any intervening claims.

6. A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then

the shortened statutory period will expire on the date the advisory action is mailed,

and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the

mailing date of the advisory action. In no event, however, will the statutory period

for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong 2/9/2007

KEVIN KIM
PRIMARY PATENT EXAMINER